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Simulation of 3-Phase 17-level Inverter Using two Cascaded Square Wave Bridge

Abdul Basit [1], Sheharyar Khan[2], Abdul Wahab[3], Kamil jalal[4], Waseem Gohar[5] and Kashif Hussain[6]

[1] School of Electrical Engineering, University of science and Technology Bannu, KPK, Pakistan
[2] School of Software, Northwestern Polytechnical University, Xian, China
[3] School of Automation, Northwestern Polytechnical University, Xian, China
[4]School of Electrical Engineering, Southeast University, Nanjing, China
[5]School of Automation Science and Engineering. South China University of Technology, Guangdong, China
[6]School of Information science and technology, Dalian Maritime University, Dalian, China

Correspondence Email: wahab.engr55@yahoo.com

Abstract: Nowadays, electronic devices are very sensible with harmonics. The need for a harmonic free and large-grade power supply is also enhanced to meet the industry's requirements. This paper presents simulation of 3-phase 17-level cascaded h-bridge inverter by using two cascaded square wave bridge. Inverters are mainly divided as single or multi-level. The multi-level fundamental switching technique is used to control the power required for electronic switches. We have presented the methodology where switching angles are calculated so that the desired fundamental sinusoidal voltage is generated from the dc sources; however, at the same time, specific high order harmonics are removed. Comparative study of different types of sinusoidal pulse width modulation (SPWM) schemes such as phase disposition (PD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) with different modulation index (Ma) are proposed to decrease total harmonic distortion (THD) up to 5.65%. MATLAB Simulink results are included to demonstrate the effectiveness of the proposed multi-level inverter.

Keywords: multi-level inverter, pulse width modulation, total harmonic distortion, modulation Index, MATLAB Simulink.

1. Introduction

Multi-level inverters [1-10] have been getting tremendous consideration in the later past years to get a higher voltage and higher power applications in industry and the household. They have an advantage over conventional 3-level inverters due to their ability to reduce the lower order's harmonic content by increasing the number of levels [1, 11, 12]. The multi-level inverters are designed to generate voltage or current waveforms having minimum harmonics[1, 13]. For high power and voltage operations, the typical 3-level inverters have a limitation in working at the higher frequency because of frequency loss and components of power electronic gadgets: parallel and serial arrangements of power switch concerning getting the power controlling current voltage. Typical 3-level inverters have a total harmonic distortion value around 60% even under ordinary working situations, leading to a more significant loss[14].

Another problem is the power quantity on AC drive operations. A multi-level inverter increases the power than the two-level inverter through the arrangement and parallel association of intensity transistors used as switches. The same is the case with the power quantity on AC drive operations. A multi-level inverter increases the power than the two-level inverter through the arrangement and parallel association of intensity transistors used as switches. In contrast, this and the 3-level inverter frameworks give similar power ratings; multi-level inverters benefit from the fact that the lower consonant segments at the output voltages could be expelled electromagnetic issues be decreased. According to all these favourable circumstances, the more significant part of the multi-level inverters' examinations are done consistently and uses fewer components[12, 14]. Multi-level inverters have been designed in many topologies, such as a diode clamp, a flying capacitor, and a cascaded h-bridge. The most efficient topology is cascaded h-bridge (CHB) topology, which has been introduced to reduce the total harmonics distortion and get the normalized power at the output source[7, 15]. The multi-level inverter is used for factory operations as an alternative when high or medium voltage is required. These inverters are usually connected in the cascaded form to make a serial array of levels. Multi-level inverter topology must comply with the factors mentioned below:

- Less number of switching components as less as possible
- It must be durable to bear higher input voltages to delivers ultra-power
- A lower switching frequency of the switching gadgets is necessary

This paper has explicitly intended to demonstrate the simulation of the 3-phase 17-level inverter by employing the h-bridge topology. There were different pulse width modulation (PWM) schemes [14, 16] like phase disposition (PD), phase opposition disposition (POD), and alternative opposition phase disposition (APOD)[4, 6] that have been implemented and compared through the FFT analysis.

2. Related Work

Multi-level inverters with cascaded H-bridge (CHB) topology [1, 2, 4, 6, 7, 11-13, 15, 17] have drawn enormous interest in heavy-duty industries and high-voltage applications in recent past years. The use of a multi-level inverter has become the right approach for high power and quality power demands. The term "multi-level" means that the n-level inverter can produce an n-voltage level rather than a 2-level inverter as in the convention "3-level inverter"[14]. The use of a 3-level inverter[16] was first proposed as a multi-level inverter. Similarly, the various multi-level inverter has been proposed, which includes the n-level of the inverter. The main idea implies in the multi-level inverter is to use several semiconductors switches to produces several voltage levels. A comparative study of three phases 5-level cascaded H bridge (CHB) topology with other topologies has been presented[7]. Asymmetric and symmetric multi-level inverters have been proposed with a novel strategy to reduce the number of switches and dc sources [13]. A case study of single-phase multi-level inverter having using cascaded H-bridge topology being presented to draw even and odd voltage levels; it has also reduced the cost and number of switches [15]. The multi-level inverter could also withdraw an input current with lower harmonics at higher and lower switching frequencies with lower switching losses and higher performance, resulting in lower THD values at the output without any filter.

Nowadays, with unprecedented development in the industry and the advent of large-scale control application devices reaching the megawatt (MW) mark, it would be challenging to connect direct power transistors to standard grids with a range of 6.9 kv. Due to these limitations, an advanced multi-level inverters class was introduced to work with high power applications.

3. Multilevel inverters (MLI's)

Multi-level inverter is an excellent source for power generation, such as photovoltaic (Solar) power inverter [18], as shown in Fig 1. We can also utilize it for power, generation, and control,

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transports, a group of systems, fans, pumps, and others. The multi-level inverter does the job of high-power delivery at lower costs and also covers the low power usage unreliable power source, solar cells (panels) and intensity gadgets get connected with the staggered inverter circuit as a reason to give us the high power, as most as often as possible and essential starting utilization of the staggered inverter is in scope, in trains as well as track-side static inverter. Other applications include power systems inverter being utilized for the dynamic separating, which gives to drive high voltage requiring engines, also used to get high voltage dc transmissions, and also capable of regular voltage variable speed drives of the engine. The inverter can manage ultra-voltages to provide high power. That's why inverters are manufactured with various switching qualities, for example, entryway thyristors, incorporated door merged transistors, and insulated gate bipolar transistors in terms of the reality that the switching combination allows to achieve higher voltages. Different topologies were implemented and observed to produce harmonic free output power[4]. The classification of the multi-level inverters has been shown in Fig 2 below. Subsequently, the yield voltage of the multi-level inverter has multi ventures produced from plenty of DC supplies. The output voltage value gets better as the number of levels increases, and the harmonics percentage decreases by increasing the ventures. On the off chance that we go into the memorable foundation of the staggered inverter, then we become acquainted with that in the 1975 idea of staggered converters has been coming into presence. The arrangement staggered inverter was proposed as a matter of first importance in 1975[19]. The isolated dc sources are responsible for generating the multi-level staircase AC voltage waveform at the output. The term MLI gets initiated with the 3-level inverter [16]. At the same time, various MLI arrangements were proposed at that time. The diode-clamped inverter was introduced in 1981, also known as NPC (Neutral Point Clamped) inverter.

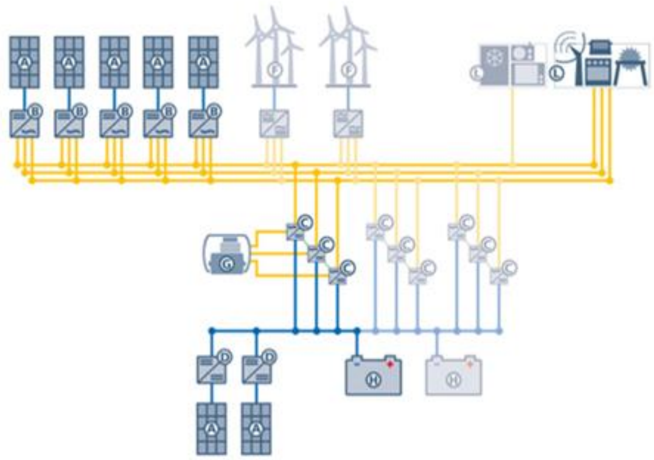


Fig 1. Photovoltaic (Solar) power inverter

The flying capacitor topology was introduced in 1992, and the cascaded multi-level topology was proposed in 1996[4]. However, the cascaded multi-level inverters were designed before, but it was not used before the 1990s. Multi-level inverters have been classified into two main categories, such as MLIs having separate and familiar DC sources, as shown in Fig 2 below. On the other hand, the MLIs having separate DC sources make cascaded topology, and familiar DC sources make diode clamped and flying capacitors MLIs. Our proposed methodology is being based on the cascaded MLIs. The usage of the cascaded multi-level inverter was in drives of the engine and for other power utilization purposes. The cascaded inverter gets a higher interest of consumers because it provides firm control over the medium voltages. The usage of the cascaded multi-level inverter was in drives of the engine and for other power utilization purposes. The cascaded inverter gets a higher interest of consumers because it provides firm control over the medium voltages. The cascaded multi-level inverter we mostly use in regenerative-type engine drives.

Some other topologies of multi-level inverters are proposed, increasing the output voltage and power, consequently increasing the number of levels. The voltage or current rating of the multi-level inverter is converted into a set of single switches. Thus, the power rating of the inverter exceeds the point of containment induced by each switching unit.

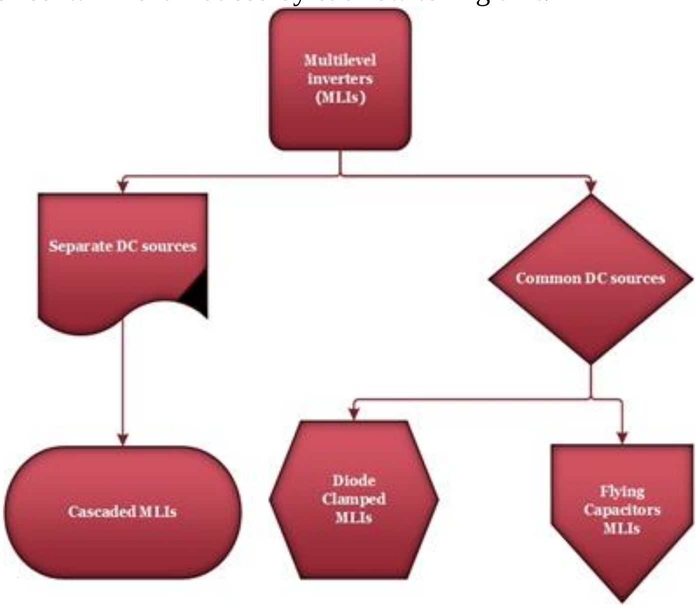


Fig 2. Photovoltaic (Solar) power inverter

A multi-level inverter's rudimentary concept is to achieve high power to use power transistors with plenty of dc supplies to transfer the power by producing the multi-level staircase signal. Solar cells, dc batteries, and capacitors are using as a DC source of the inverter. A multi-level inverter is superior to the typical binary level inverter because of pulse width modulation (PWM) techniques[14]. Some highlighting features of multi-level inverters are as follow:

- Quality of multilevel staircase waveform: Not only the multi-level inverter output waveform eliminates the blending, but somehow it reduces the voltage over time stresses, so the electromagnetic similarities get reduced
- Common-mode (CM) voltage: Multi-level inverter provide lesser common-mode (CM) voltage, so the load connected with the inverter make it safe from any damage
- Input current: These inverters draw current from the source with minimum possible bending at the edges
- Switching Frequency: These inverters operate at both low and higher switching frequencies with pulse width modulation. At low switching frequency, the inverter is more productive

4. Proposed Methodology

a) Cascaded Square Wave h-bridge:

A multi-level Inverter is an electronic gadget that integrates a coveted AC voltage from a few DC voltage sources[4, 18]. Multi-level inverters are a vital topic for research over the most recent quite a while, where the DC levels were viewed as almost identical because these are either batteries, solar panels, or others. Multi-level inverter of having cascaded h-bridge topology is better than the diode clamped inverter and flying capacitor inverter, as it needs less part in each switching level. A power electronic circuit consists of four IGBTs used as a switch, limiting the current flow to the connected load. The schematic diagram of a conventional h-bridge is shown in Fig 3 as each switch is connected to a single DC source The grouping of switches and condensers is called an h-bridge with an insulates DC voltage source in cascaded h-bridge multi-level inverter. The switching pattern is being given in Table 1. It produces three-level output voltage waveforms. Here we give one dc source as an input supply, two not gate on diagonal, and two direct input signals to drive the gate accordingly to produce three-level output waveforms.

Table 1. Switching pattern of cascaded h-bridge

Symbols	Switching states			
V output	S1	S2	S3	S4
VDC	1	0	0	1
1	1 0	1 0	0 1	0 1
VDC	0	1	1	0

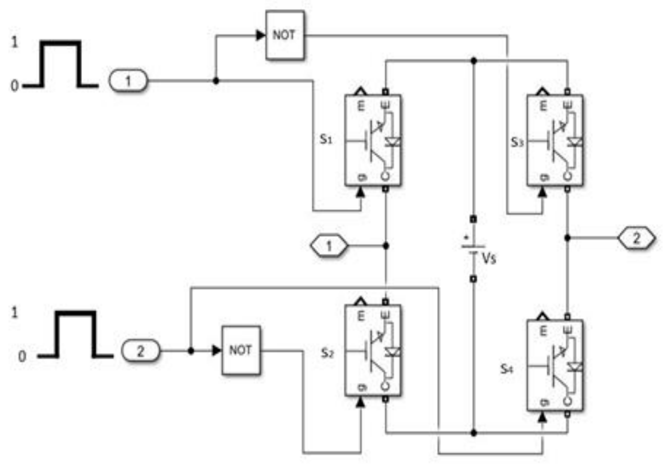
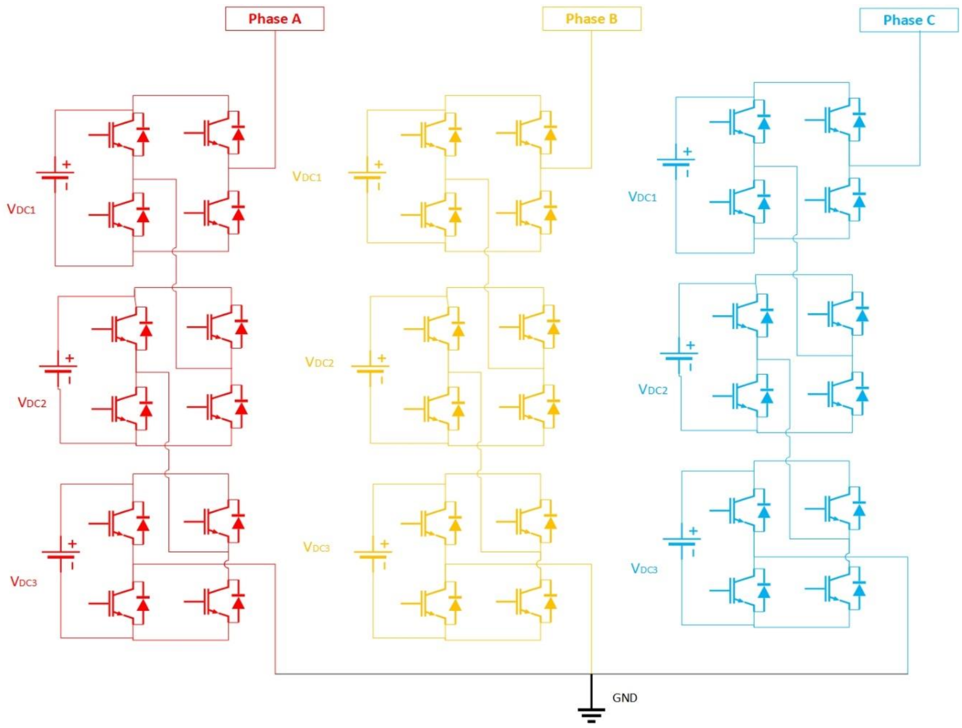
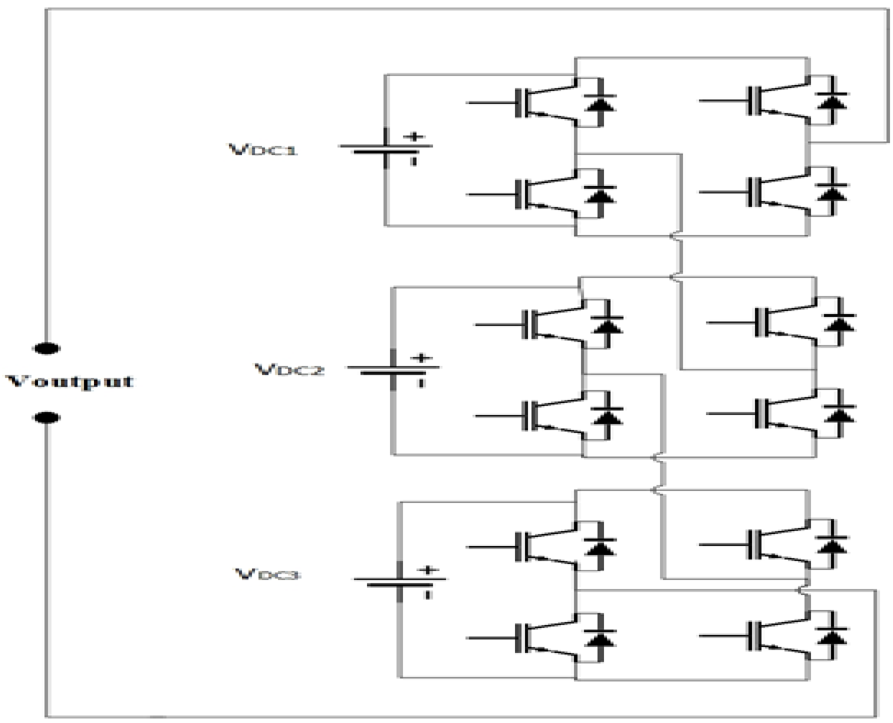


Fig 3. Common h-bridge circuit

The h-bridges are primarily used in inverters design. Below is the circuit diagram of a common h-bridge. This h-bridge generates a square wave of voltage at the load connected. Two isolated DC sources are auxiliary to the two transformers linked to AC control utility. Here separate DC sources connected to each h-Bridge in cascade is the critical point. The Cascaded multi-level inverter utilizes h-bridges having separate DC sources in a manner that functions to deliver high AC power. A seven-level three-phase and single-phase cascaded h-bridge system appears in Fig 4 (a) and (b) underneath, where each stage leg comprises three h-bridges cells fuelled by three segregated *VDC* of an equivalent rating of *30 Volts*. The cascaded h-bridge (CHB.) inverter can deliver a stage voltage with seventeen voltage levels having a *240V* peak value, and for the seven levels, the voltage is 90V.



(a)



(b)

Fig 4. (a) Circuit diagram of cascaded h-bridge (Three-phase 7-level Inverter). **(b)**Single-phase 7-level inverter

Figure 4(a) shows a 3-phase 7-level cascaded h-bridge inverter, each phase is shifted by 120 degrees to generate 7-level ac voltage, and Fig 4 (b) represents a single-phase 7-level cascaded h-bridge inverter circuit. Each bridge produces 3-level, so in three bridges produce 9-level, but the reference level is standard for each bridge, so the total levels become 7-level. The formula for the calculation of the number of CHB bridges is given by (1):

$$N = \frac{m-1}{2} \quad (1)$$

b) Simulation of 3-Phase 17-Level Inverter

I. Modulation Schemes

Multi-level Inverters generate an AC voltage of varying amplitude and recurrence (frequency). We have employed the sinusoidal pulse width modulation (SPWM) scheme. The output waveforms of PWM inverters are far better than the square-wave inverters. The SPWM inverters are regularly utilized in AC motors having varying speeds. Sinusoidal pulse width modulation (SPWM) [4, 6] innovation is utilized in Inverters to give a consistent output voltage of *110V* or *230Volts* AC regardless of the load. The Inverters dependent on the SPWM innovation are better than the traditional inverters. The modulation index (*Ma*) plays a vital role in the SPWM. It relates the inverter's dc-interface voltage and the extent of shift voltage (fundamental part) output by the inverter. The baseband signal frequency is lower relative to the carrier wave frequency. The carrier-based modulation plans for multi-level inverters can be, for the most part, grouped into two classifications, such as phase-shifted and level shifted SPWM [6, 20, 21], as shown in Fig 5 below.

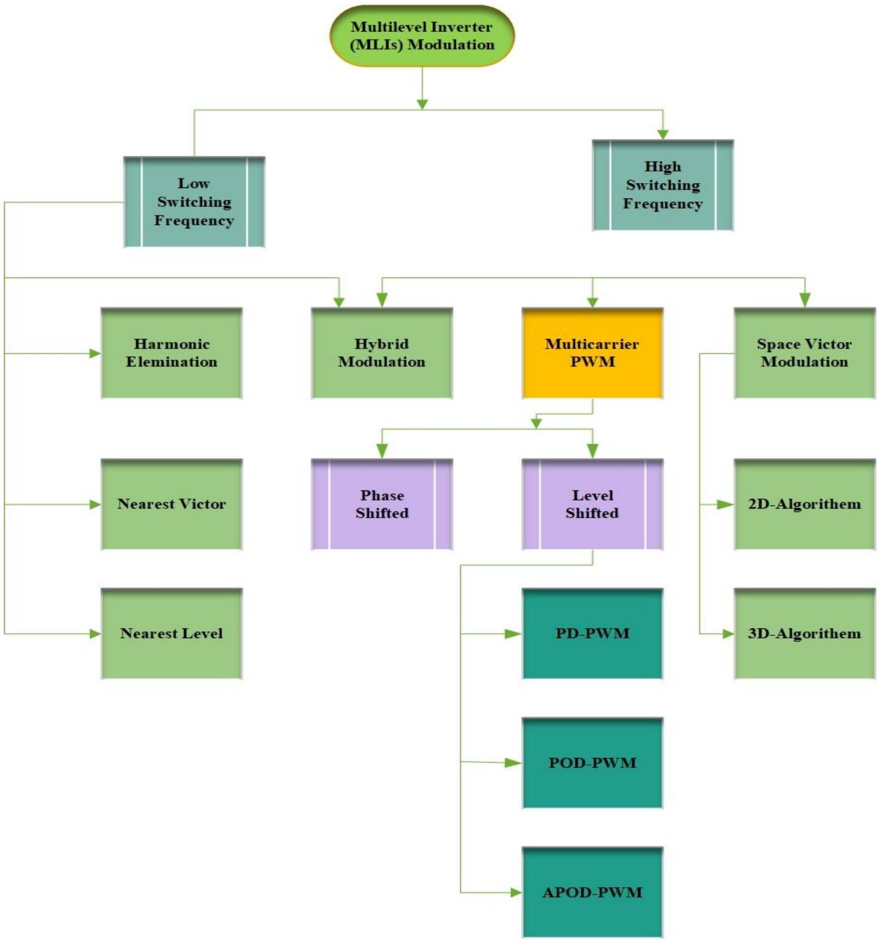


Fig 5. Classification of modulations schemes for MLIs

II. Phase Shifted PWM

Each pair of switches has a carrier signal in this framework, moving to another step. Overall, a multi-level m voltage inverter requires *(m-1)* triangular voltage carriers. Both the triangular carriers have this method the same frequency and the same maximum amplitude, but a phase shift φ_{cr} occurs between two neighboring carriers Signals which is given by (2);

$$\varphi_{cr} = \frac{360}{m-1} \qquad (2)$$

The modulating signal is usually three-phase sinusoidal with customizable amplitude and frequency. The gate signals are created by comparing the modulated signal with the carrier's signals. If the module signal is above the carrier, the higher switch and the lower switching's on. Amplitude and modulation index (*Ma*) and frequency modulation index (*Mf*) also apply here. It should be remembered that the phase-shifted modulation schemes cannot be used for diode-clamped multi-level inverters because they have no switching consistency [20].

III. Level Shifted SPWM

Similar to the phase-shifted modulation scheme, it has an m-level inverter using a level-shifted multi-carrier modulation scheme that includes *(m-1)* triangular carriers, all of which have the same frequency peak-to-peak amplitude. The triangular carriers are vertically organized in such a way that the bands they occupy are continual. The frequency modulation index remains the same as the phase-shift modulation scheme, whereas the amplitude modulation index is given by (3) ;

$$M_a = \frac{V_m}{V_{cr(m-1)}} \qquad (3)$$

Whereas *Ma* is the modulation index, *Vm* and *Vcr* are the peak amplitudes of modulating and carrier signals simultaneously. Similarly, *m* represents the number of levels of an inverter [20].
However, both the modulation plans can be applied to cascaded h-Bridge inverters. But, our main concern in this paper is on the level-shifted SPWM technique, and we've applied the level-shifted SPWM signals as input to the 17-level 3-Phase inverter as the circuit diagram of SPWM is shown in Fig 6 below, where each repeat sequence is compared to the sinusoidal signal through the comparator to produce the signals for the required gates. There are the following three level-shifted SPWM schemes for the simulation of our proposed MLI methodology, such as PD, POD, and APOD-PWM [6, 7, 17].

1) *Phase Disposition (PD-PWM)*

PD-PWM scheme has all the carrier waves at a 0° phase shift, or we can say that all carrier signals are in the same phase. The output waveform for PD-PWM is shown in Fig 7(a). We have got the least value for this plan as compared to the other two POD and APOD-PWM.

2) *Phase Opposition Disposition (POD-PWM)*

With In the POD-PWM scheme, as shown in Fig7 (b), all carrier waves are above the zero-reference level and have the same phase, while all carrier waves below zero have a 180-degree phase shift for the above zero reference level waves.

3) *Alternative Phase Opposition Disposition (APOD-PWM)*

Equations are consecutively out of phase from each other. There is a 180-degree phase shift among each carrier wave, or we can say All the carriers above or below the zero-reference level are out of phase, having 180 degrees phase shift, as shown in Fig 7 (c).

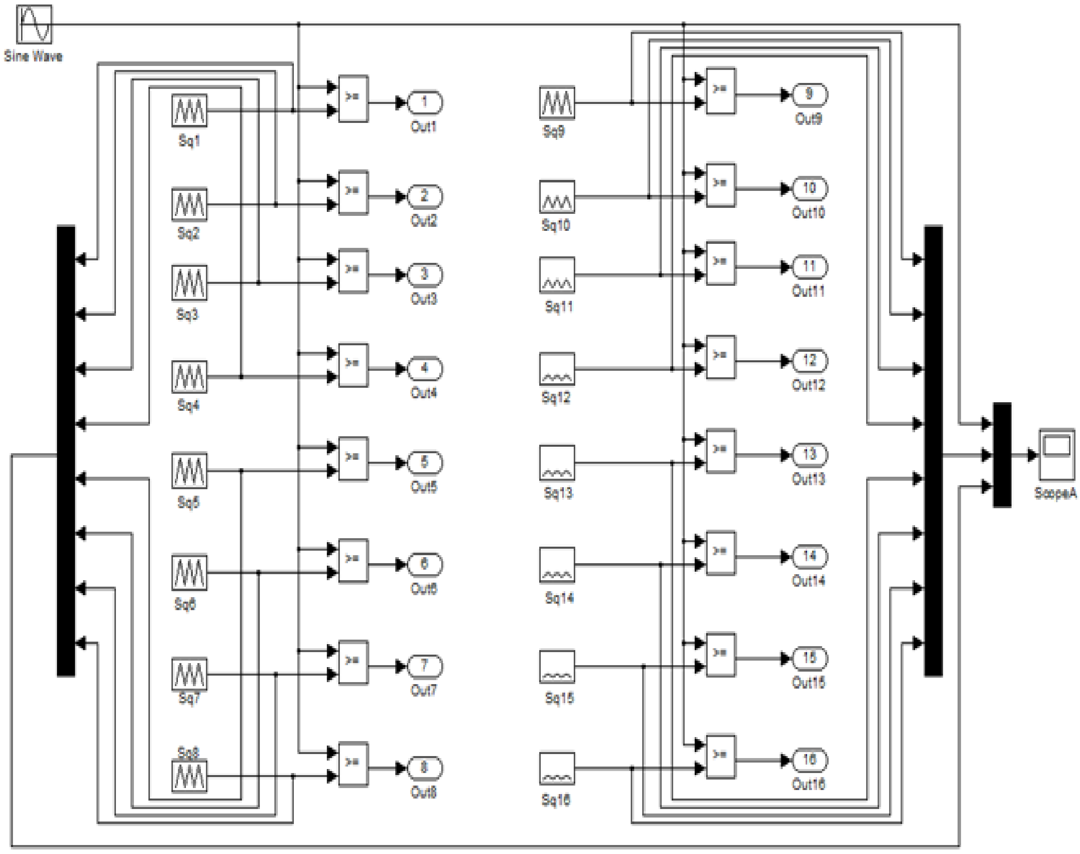
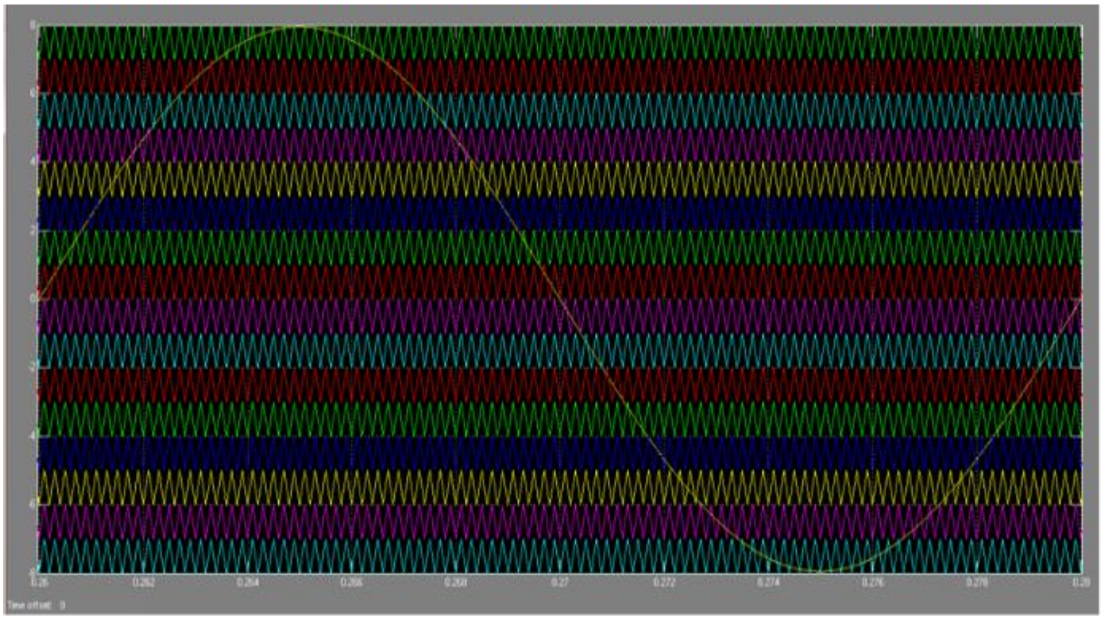
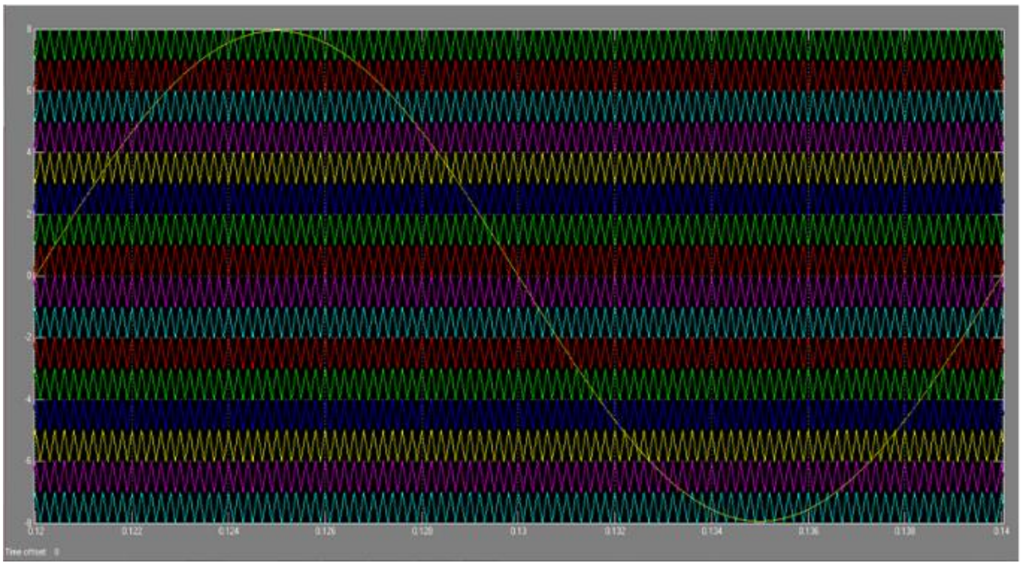


Fig 6. Sinusoidal pulse width modulator circuit



(a)



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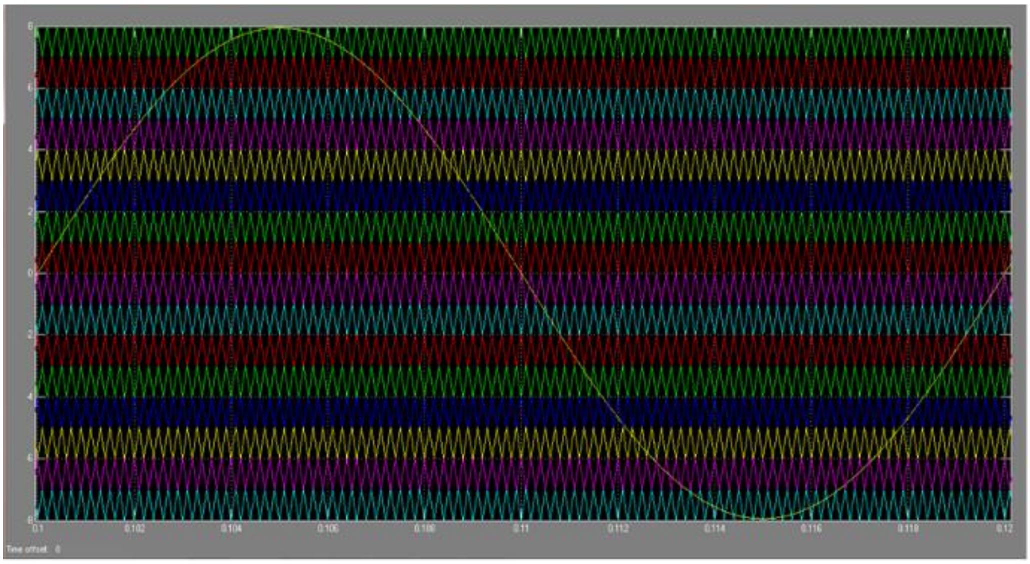

(c)

Fig 7. (a) PD-PWM**, (b)** POD-PWM and **(c)** APO-PWM output waveforms

5. Modelling and Simulation Results

To design a 3-phase 17-level Inverter, the modulating signal in each phase must have a 120° phase shift. As shown in Figure 8, the proposed gate driver block diagram for 3-phase 17-level connected with three-phase loads and proposed circuit diagram has been presented in Fig 9, the same carrier frequency fc and Ac amplitude are valid on all carrier waves. At the same time, the modulating signal has an f_m frequency and an Am amplitude. The fc must be three times f_m integral multiples. (Frequency modulating). For all three phases of the inverter, it is crucial to modulate the signal as if each phase is divided by 120 ° [22]. The carrier waves and the (modulating) signals are studied, and if the amplitude of the baseband (modulating) signal is more dominant than that of the transporter signal, it is the output characteristic of the positive half-cycle, and the comparator's output is large. For this reason, the comparator's output is high and null generally for this negative half period if the modulating signal is less than the carrier signal.

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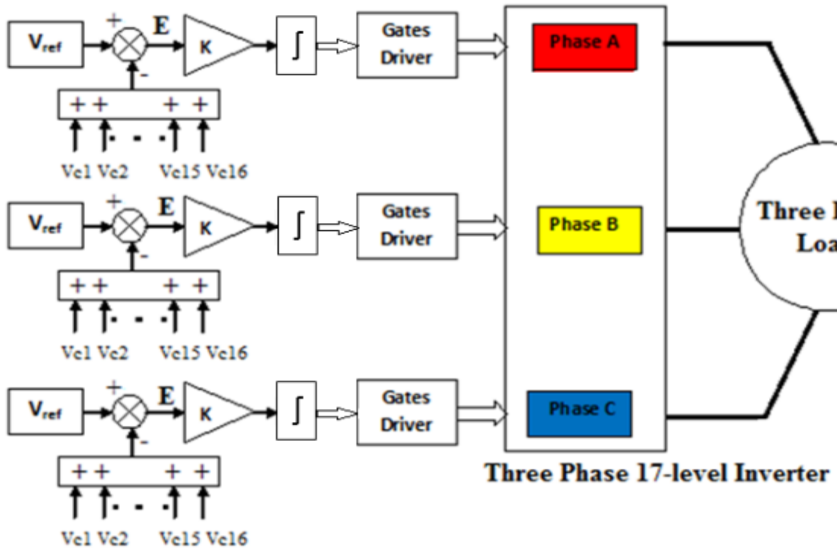


Fig 8. Proposed gate drives block diagram

As it is clear from Fig 8 that for 3-phase 17-level cascaded h-bridge, each phase produces 17-level on their output waveforms. Simulation for all three types of level shifted Sinusoidal PWM were performed, namely PD-PWM., POD-PWM, and APOD-PWM, which are shown in the above Fig 7 (a),(b), and (c). The internal Simulink model of the proposed inverter is shown in Fig 9 below. We have V_{phase} and V_{LL} are given by (4), (5);

$$V_{Phase} = V_{DC} \times N \quad (4)$$

$$V_{LL} = \sqrt{3} \times V_{Phase} \quad (5)$$

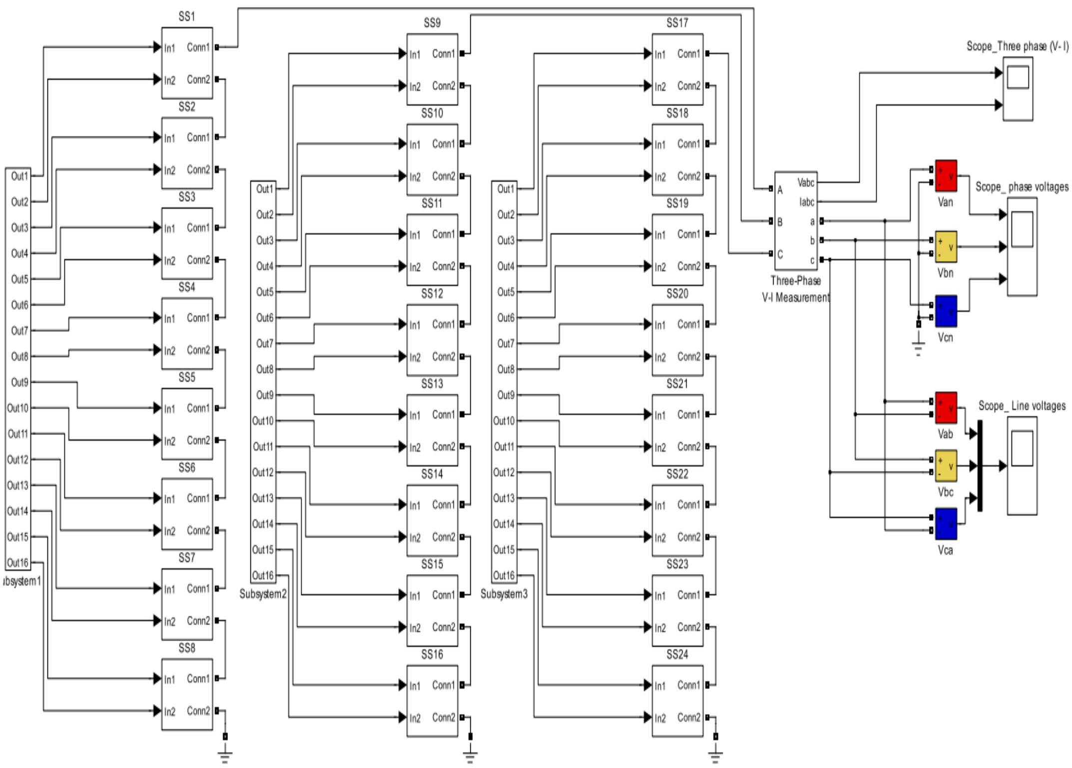
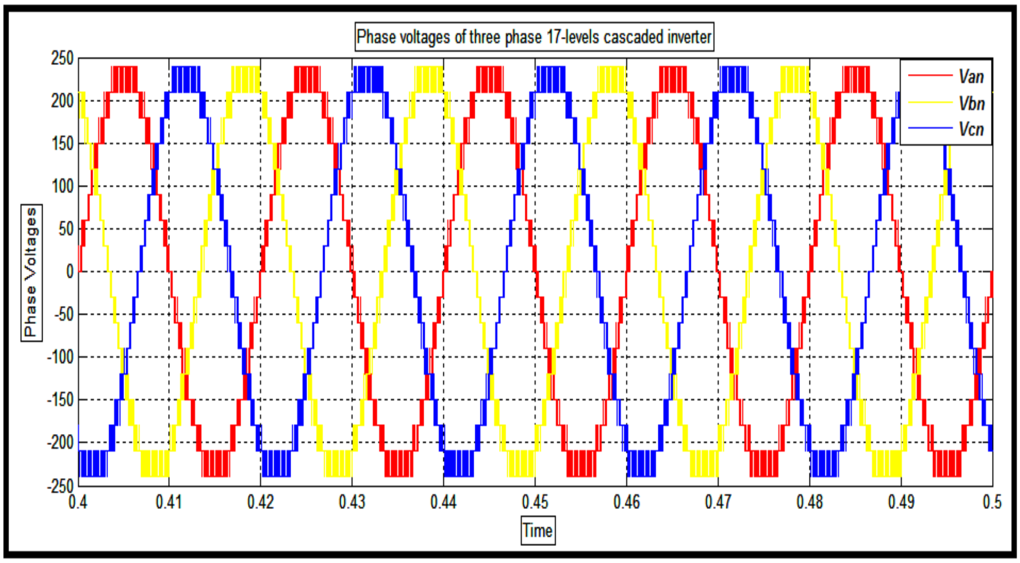
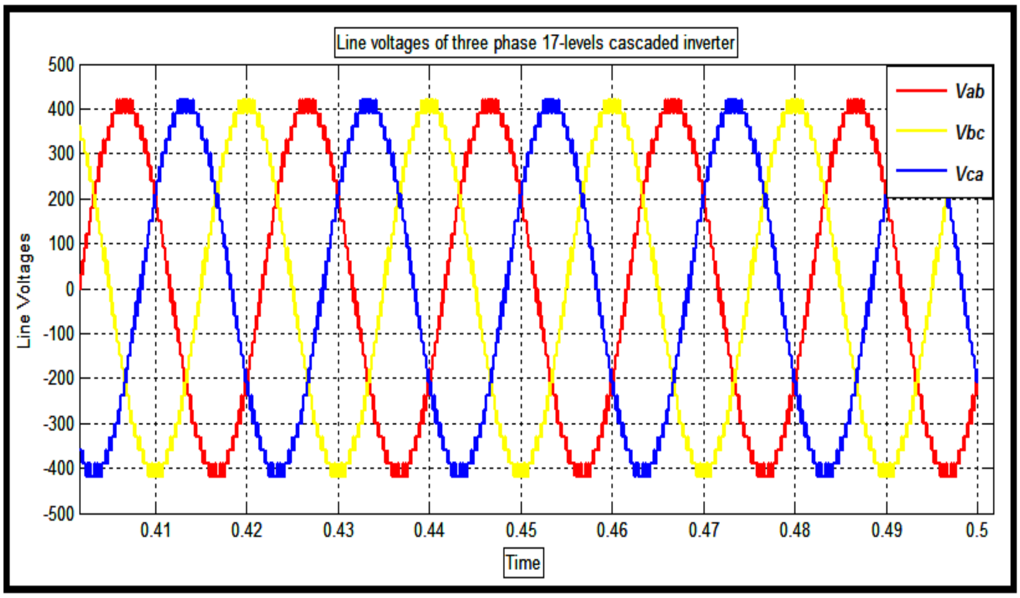


Fig 9. Proposed circuit diagram of 3-phase 17-level inverter

Whereas Eq (4) and 5 shows phase and line voltages. As we have *VDC= 30V* and number of bridges (*N=8*), we get *Van=240V* as our output phase voltage; the same case is for the *Vbn* and *Vcn*, as shown in Fig10 (a) below. Similarly, the line voltage is the √3 and phase voltage product, so we get *Vab=415.69V* in a similar way to get *Vca* and *Vbc*. The output waveform for the line voltage has been shown in Fig 10(b) below.



(a)



(b)

Fig 10. (a) Phase voltages at fsw =10 kHz, M_a= 0.998, **(b)** Line voltage (V_{LL}) waveform

(f_{sw} =10 kHz and M_a = 0.998

Table 2. %THD of line and phase voltages for different spwm (modulation indices range without levels reduction or pulse dropping)

M_a	V_{LL} % THD			V Phase % THD		
	PD	POD	APOD	PD	POD	APOD
0.538	8.71	13.88	13.65	15.01	15.96	16.15
0.593	7.03	12.43	11.06	13.54	14.84	14.83
0.630	7.91	12.49	10.97	13.25	14.59	14.47
0.681	6.94	11.25	10.09	11.96	13.52	13.38
0.733	6.28	10.36	9.12	11.5	12.56	12.56
0.780	6.53	10.20	9.59	10.42	12.12	12.00
0.840	5.87	8.95	8.46	10.16	12.56	11.30
0.880	5,78	8.91	7.88	9.41	11.13	11.15
0.944	5.40	8.41	7.65	8.64	10.61	10.52
0.994	5.58	8.03	7.82	8.19	10.09	10.19
0.998	5.65	8.14	7.86	8.19	10.08	10.19
1.00	5.63	8.20	7.80	8.18	10.11	10.18
1.068	5.57	6.49	6.81	8.42	9.29	9.38
1.107	5.90	6.22	6.61	9.67	9.59	9.36

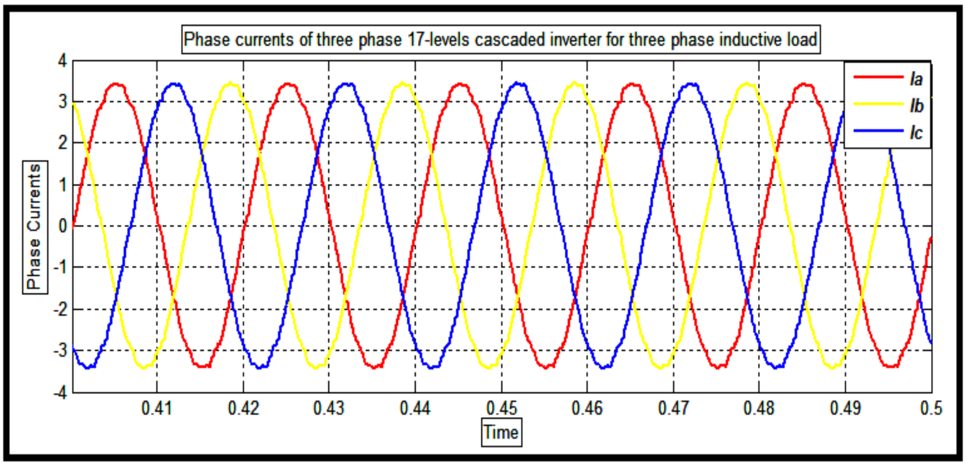


Fig11. Phase currents for inductive load (Δ) at f_{sw} =10 kHz and M_a = 0.998

Table 3. %THD of line and phase voltages for different spwm (modulation indices range without levels reduction or pulse dropping)

Elements	Ma	R-L(Δ) Load	R-C (Δ) Load	RLC(Δ) Load	R(Δ) Load
R=200Ω L=50mH C=50μF	0.50	2.40	15.08	7.86	12.09
	0.60	3.74	12.16	8.08	8.69
	0.70	2.77	11.74	7.93	8.65
	0.88	3.05	10.29	8.25	6.43
	0.99	2.03	9.95	7.23	6.41
	1.00	2.05	10.01	7.29	6.48
	1.06	2.08	9.25	7.41	5.28
	1.10	2.63	9.70	7.80	5.72

After applying different modulation index (Ma) values, we have concluded that it directly affects the line and phase voltages in terms of THD. As shown in Table 3, that when we increase the value of Ma from 0.538 to 1, the THD value decreases; after much evaluation on three schemes PD, POD and APOD-PWM, we have discovered that PD gives us the least THD and reliable source of AC voltage as compared to other two schemes.

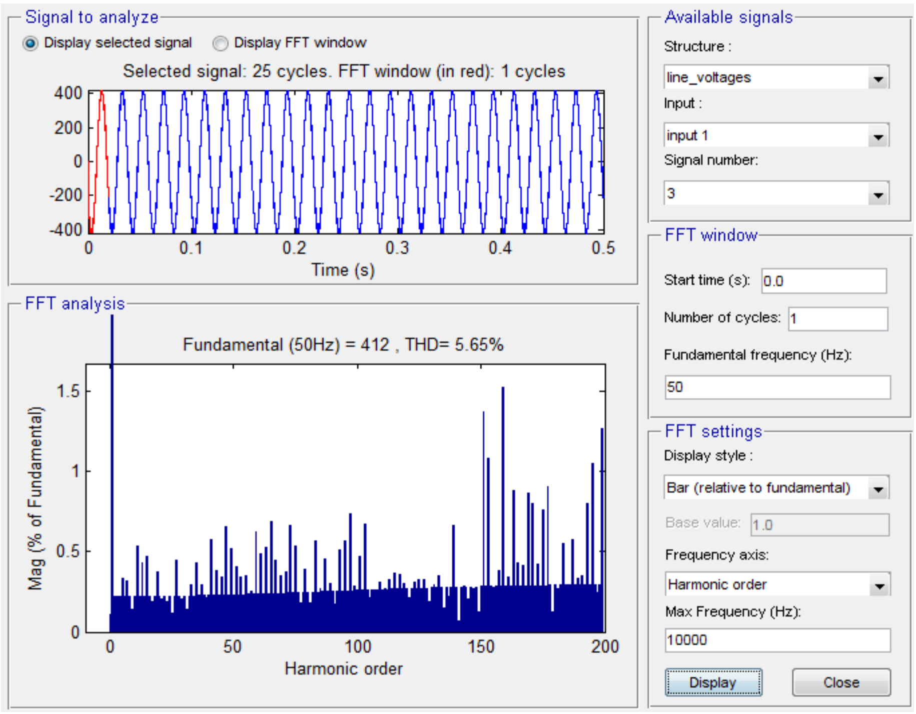


Fig 12. Harmonic spectrum of line voltage

The modulation index for reference voltage is given by Eq (6) below:

$$M_a = \frac{V_{ref}(p-p)}{(m-1)V_c} \quad (6)$$

Ma (min) for m-level prior to the pulse dropping is*:*

$$M_{a(min)} = \frac{(m-3)}{(m-1)} \quad (7)$$

Similarly, the THD is being calculated at the different *Ma* values by applying different loads such as resistive inductive(*R-L(Δ))*, resistive capacitive (*R-C(Δ))* or a combination of all three resistive inductive and capacitive (*RLC(Δ)),* or pure resistive (*R (Δ))* as shown in Table 2 .it is being concluded that when we increase the value of *Ma,* the THD of the phase current inversely decreases. We got the least values for all loads at *Ma=1.10* but got least among all for *R-L (Δ)* load. The values of the *R*, *L*, and *C* were kept constant for all the experiments. Similarly, the output waveform of phase currents such as *Ia*, *Ib*, and *Ic* was derived using inductive loads with *fsw=10Khz* and *Ma=0.998*, as shown in Fig11.Later on, Fast Fourier Transforms (FFT) analysis has been performed, as shown in Fig 12, the total harmonics distortion (THD) shown for the proposed model. From FFT analysis, we understood that when we increase the number of levels, it decreases %THD.

6. Conclusion

3-Phase CHB 17-level Inverter with a diminished number of power electronics gadgets and separate DC supplies have been designed and simulated. All the results of this paper are performed using MATLAB/Simulink. The execution of the proposed 17-level CHB inverter is researched in depth. The modulated waveforms and the %THD are examined through three different modulation schemes and compared. By applying three different modulation schemes to a 3-phase 17-level CHB inverter, it resulted in the least %THD and better harmonic profile for all modulation indices at the phase disposition (PD) modulation method. It provides a confined range of modulation indices for specific load with qualitative output waveforms. It is a very effective method for inductive load with the lowest THD as compared to POD-PWM and APOD-PWM methods. This proposed inverter framework offers the benefit of lower harmonic contents at the output. High switching frequency gadgets at low voltage and low-frequency devices can be utilized at a higher voltage. This statement concludes that this CHB Inverter topology can be utilized for every day and ultra-power purposes. Our main objective is to provide output AC voltage with minimum possible harmonics. In our proposed work, the system is 94% linear.

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